TEXAS INSTRUMENTS

TLV1570 Evaluation Module

User's Guide

1998

Mixed-Signal Linear Products

SLAU024

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Preface

Read This First

About This Manual

This user's guide describes the characteristics, operation, and use of the 10-bit TLV1570 analog-to-digital converter (ADC) evaluation module (EVM).

How to Use This Manual

This document contains the following chapters:

- Chapter 1 – Introduction
- Chapter 2 – Analog Configuration
- Chapter 3 – Digital Interface
- Chapter 4 – Hookup With TMS320C203 DSP
- Chapter 5 – Technical Data
- Chapter 6 – Connector and Jumper Description
- Chapter 7 – Schematic, Board Layout, and Parts List

Information About Cautions

This book contains cautions.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

CAUTION

The information in a caution is provided for your protection. Please read each caution carefully.

Trademarks

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Chapter 1

Introduction

This chapter gives an overview of the TLV1570 EVM.

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1.1 TLV1570 EVM Kit

The TLV1570 EVM kit contains the following items:

- One EVM
- This manual
- TLV1570 data sheet
- TLV5616 data sheet
- TLV2231 data sheet

1.2 Description

This EVM provides a platform for prototyping the TLV1570 in a laboratory environment. The TLV1570 is an 8-channel, 10-bit, 1.25-mega-samples-per-second (MSPS) ADC with a 4-wire serial interface. It is designed to be compatible with 3-V and 5-V systems and can be connected without glue logic to Texas Instruments (TI™) digital signal processors (DSPs) and microcontrollers with a serial-port interface (SPI). With the EVM, it is possible to quickly determine how the TLV1570 can be used in a signal-processing system with minimal development effort.

In addition to the ADC, there are several components that help evaluate the function of the TLV1570:

- 12-bit digital-to-analog converter (DAC) TLV5616 (U3). The output of the DAC can be routed to a channel of the ADC (loopback feature).
- External voltage reference circuit that can be used for the ADC and the DAC. The voltage can be adjusted by replacing the default zener diode (D1).
- Operational amplifier (U4) between the multiplexer output pin and the ADC input pin. The gain is selectable by changing two resistors (default gain: 1.0).
- Potentiometer (R2) that can be used to generate an input voltage within the range of the converter

Test points across the printed circuit board (PCB) allow easy measurements on the analog signal chain and the digital interface signals. The interface signals are buffered to protect the ADC.

To achieve optimal signal quality, the PCB consists of four layers: two signal layers and two power-plane layers. The power-plane layers are divided between analog and digital. A separate prototype area can be used to add extra signal-conditioning circuits.

Chapter 2

Analog Configuration

This chapter describes the possible analog input and output configurations, signal conditioning, and voltage reference.

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2.1 Analog Configuration

The EVM has eight analog inputs (CH0–CH7) and one analog output. CH1–CH6 are directly accessible on J1 (pins 3, 5, 7, 9, 11, and 13). CH0 can be switched between J1 (pin 1) and the output of the onboard DAC via JP2. The input of CH7 can be either J1 (pin 15) or the wiper voltage of the potentiometer, depending on the setting of JP1. With the DAC or the potentiometer, it is possible to evaluate the TLV1570 without need for an external signal source.

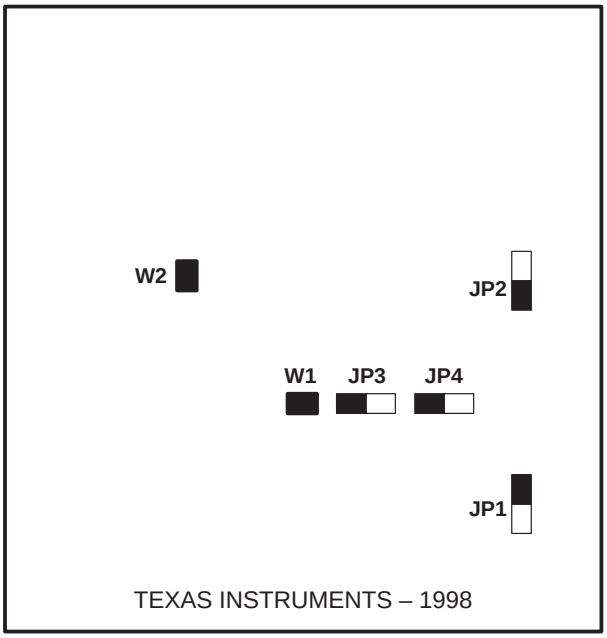
Table 2–1. J1 Pin Assignments

Pin No.	Name	Pin No.	Name
1	CH0	2	AGND
3	CH1	4	AGND
5	CH2	6	AGND
7	CH3	8	AGND
9	CH4	10	AGND
11	CH5	12	AGND
13	CH6	14	AGND
15	CH7	16	AGND
17	AGND	18	AGND
19	OUTA	20	AGND
21	FS/OUTB	22	AGND
23	CH7	24	AGND

2.2 Jumpers

The setting of a jumper is either UP, DOWN, RIGHT, or LEFT. This refers to the position of the jumper when looking at the EVM board, so that the text TEXAS INSTRUMENTS – 1998 is readable as shown in Figure 2–1.

Figure 2–1. EVM Board Jumper Settings



The jumper settings in Figure 2–1 are the default settings. The jumper settings are:

Jumper	Default	Description
JP1	UP	CH7 connected to J1, pin 15
	DOWN	CH7 connected to R2
JP2	UP	CH0 connected to DAC output
	DOWN	CH0 connected to J1, pin 1
JP3	RIGHT	AIN connected to amplifier U4
	LEFT	AIN connected to JP4
JP4	RIGHT	MO connected to amplifier U4
	LEFT	MO connected to JP3
W1	SET	Onboard reference used
	CLEARED	Onboard reference not used
W2	SET	Default (TV5616 compatible)
	CLEARED	Reserved (TLV5618A compatible)

2.3 Onboard Signal Conditioning

The multiplexer output of the TLV1570 is not directly connected to the input of the converter. That makes it possible to insert a signal-conditioning circuit between the multiplexer and the ADC. On the EVM, an amplifier [TLV2231 (U4)] can be inserted in the signal path (determined by JP3 and JP4). The default gain of the amplifier is 1.0, but can be changed with R3 and R4 (as shown in the following equation).

$$G = 1 + \frac{R3}{R4}$$

The SMA terminal can be used to connect the output of a function generator directly to the input of the ADC. It is possible to set the input impedance to the required value (R19). However, if the signal is routed via the multiplexer, R19 should be left open to avoid errors due to the current through this resistor.

Jumper	Default	Description
JP3, JP4	Both RIGHT	Amplifier between multiplexer and ADC
	Both LEFT	Multiplexer connected directly to ADC

2.4 Eight-Channel Direct Operation

In this mode, all eight channels of the ADC are accessible via J1. For this, both JP1 and JP2 must be switched to the following positions:

JP1 UP
JP2 DOWN

2.5 Variable dc Voltage on Channel 7

To test the basic function of the ADC, the potentiometer R2 provides a dc voltage between 0 V and the reference voltage. JP1 connects the wiper of the potentiometer to channel 7.

JP1 DOWN

2.6 Loopback Mode on Channel 0

The onboard DAC (TLV5616) is used to run the board in a loopback mode. The voltage, generated by the DAC, is connected to channel 0 with JP2.

JP2 UP

2.7 Voltage Reference

There are three ways to generate the voltage reference:

- Onboard reference
- External reference
- Internal reference of the TLV1570 (See TLV1570 data sheet, literature number SLAS169. The internal reference cannot be used for the onboard DAC.)

2.7.1 Onboard Reference

To use the onboard voltage reference, W1 must be set. The reference voltage is generated by D1, R5, and U5. The Zener diode (D1) determines the voltage, which is buffered by U5 and connected to the reference input of the TLV1570. To get the same full-scale range, the reference voltage is divided by two (R17, R18) before it is applied to the TLV5616 (the DAC has a built-in 2× amplifier).

2.7.2 External Reference

To use the onboard voltage reference, W1 must be removed from the board. The reference voltage must be supplied on pin 23 of J1. To get the same full-scale range, the reference voltage is divided by two (R17, R18) before it is applied to the TLV5616 (the DAC has a built-in 2× amplifier).

CAUTION

The external reference voltage must not exceed the supply voltage by more than 0.3 V.

Chapter 3

Digital Interface

This chapter describes the digital interface of the EVM. It should be used together with the TLV1570 and the TLV5616 data sheets.

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3.1 Digital Interface

The digital interface consists of six signals that are accessible through J2:

- Serial clock (SCLK)
- Data in (DIN)
- Data out (DOUT)
- Frame synchronization (FS)
- Chip-select ADC (/CSAD)
- Chip-select DAC (/CSDA)

The pin assignments of J2 (see Table 3–1) are compatible with the WYLE TI C2xx Development System, featuring a TMS320C203 DSP. J2 can be connected directly to JP3 on the WYLE board. /CSAD is then connected to IO0 of the TMS320C203 and /CSDA to IO1. The positive power supply must be hardwired to pin 26, as the WYLE board does not provide a signal on pin 26 of JP3 (not used).

Both converters [TLV1570 and the onboard DAC (TLV5616)] have a TMS320-compatible serial-interface timing. The active device is determined by two chip-select signals; /CSAD for the TLV1570 and /CSDA for the TLV5616. Usually, one chip-select signal always should be high to ensure proper signal routing. However, no bus conflict occurs if both signals are low (not recommended).

Table 3–1. J2 Pin Assignments

Pin No.	Name	Pin No.	Name
1	NC	2	NC
3	NC	4	NC
5	NC	6	NC
7	NC	8	NC
9	NC	10	NC
11	NC	12	NC
13	/CSAD	14	/CSDA
15	NC	16	NC
17	CLKOUT	18	NC
19	DIN	20	FS
21	CLKIN	22	DOUT
23	FS	24	CLKIN
25	GND	26	3V–5V

Chapter 4

Hookup With TMS320C203 DSP

This chapter gives an example how to use the EVM with a TMS320C203 DSP.

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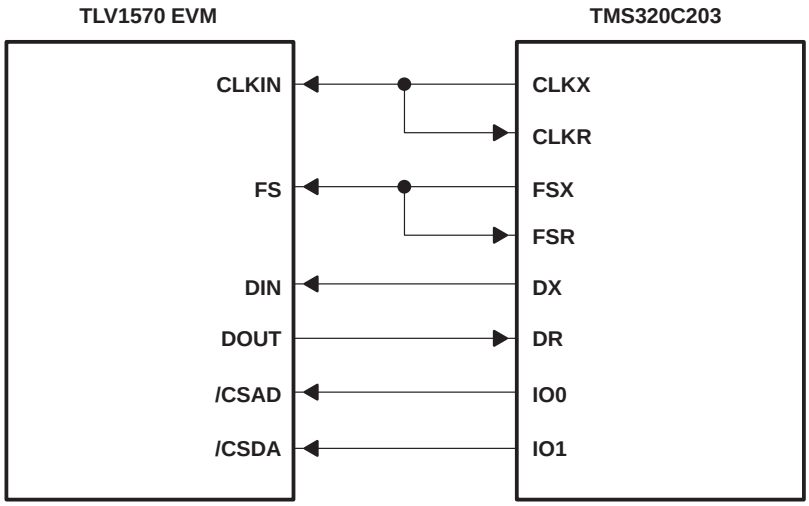
4.1 Example Hookup With TMS320C203 DSP

This example shows how to use the TLV1570 EVM with a TMS320C203 DSP. As both converters on the board (TLV1570 and TLV5616) are compatible (without glue logic) with all TI DSPs with serial interface, the hardware connections of the serial interface are the same as the other DSPs.

Figure 4–1. Example Hookup With TMS320C203 DSP



No external circuitry is needed to check out the operation of the TLV1570 (except a power supply). The following shows how to program the TLV1570. In this example, the TLV1570 converts data continuously and stores the result in a 256-word (16-bit) block within the memory of the TMS320C203 system. The time base is generated by the timer interrupt. In the interrupt handler routine, the DSP reads the last conversion result and stores it in the next address within the memory block. When 256 words are stored, the DSP starts at the beginning of the block again.

The program consists of three parts:

- Initialization (from address `start` to address `loop`)

  In this block, IO0, which provides the chip-select signal for the TLV1570, is configured as an output and driven low. The TMS320C203 timer is set up and the registers, which are used to access the data buffer, are initialized.

- Idle loop (address `loop`)

  The whole program is interrupt driven. When not in the interrupt service routine, the DSP is idle.

- TINT_handler

  In this interrupt service routine, the DSP reads the conversion result from the ADC using the serial port and stores it in memory.

4.2 Transfer Program

```
;-----------------------------------------------------------------
;File:            TLV1570.asm
;Description:     Transfers 256 Samples from TLV1570 to C203 DSP
;Version:         1.0
;Date:            10–16–1998
;Copyright:       Texas Instruments Inc.
;-----------------------------------------------------------------
SDTR       .set    0fff0h      ; sync port data reg
SSPCR      .set    0fff1h      ; sync port control reg
WSIZE      .set    00100h      ; size of waveform [words]
IFR        .set    00006h      ; interrupt flag register
IMR        .set    00004h      ; interrupt mask register
TIM        .set    0fffah      ; timer counter register
PRD        .set    0fff9h      ; timer period register
TCR        .set    0fff8h      ; timer control register
IOSR       .set    0fff6h      ; IO status register
ASPCR      .set    0fff5h      ; asp control register

           .entry
           .ps     00000h      ; reset
           b       start
           .ps     00006h      ; timer interrupt
           b       TINT_handler

           .ds     00800h      ; start of data
sio_ini    .word 1100000000111110b        ; Free/Soft = 11; free run
                               ; FT1,FT0,FR1,FR0 = 0; no FIFO
                               ; Transmit enable, Receive enable
                               ; internal FS, internal CLK, burst mode
aux        .word   00000h      ; auxiliary register
wave       .block  WSIZE       ; buffer for wave data
           .ps     01000h      ; the program begins @ 1000h
start:
           setc    INTM        ; disable interrupts
           ldp     #00010h     ; our data starts @ 00800h

           splk    #0E0C1h, aux
           out     aux, ASPCR  ;configure IO0 as output
           splk    #018h, aux
           out     aux, IOSR   ;drive IO0 low (set /CSAD, select TLV1570)

           splk    #00010h, aux
           out     aux, TIM    ; timer count value
           out     aux, PRD    ; timer reload value
           splk    #00c00h, aux
           out     aux, TCR    ; timer start

           out     sio_ini, SSPCR          ; initialize serial interface

           lar     AR1, #wave  ; AR1 points to wave memory
           ldp     #00000h                 ; IMR is located in page 0
           splk    #00024h, IMR            ; unmask timer interrupt
           ldp     #00010h                 ; switch back to our data page
           clrc    INTM                    ; enable interrupts
           nop

loop:      idle
           b       loop
```

```
TINT_handler:
          splk   #0000001110000000b, aux
                              ; Normal operation
                              ; high speed selected
                              ; no auto scan
                              ; input channel: 7
                              ; external reference
                              ; auto power down disabled
                              ; linearity optimized for 5V
          out    aux, SDTR
          mar    *, AR1       ; select data pointer
          in     *+, SDTR     ; store ADC result in wave memory (AR1*)
          lar    AR0, #wave + 00100h     ; AR0 points to end of wave memory
          cmpr 1 ; AR1 < AR0 ?
          bcnd wave_not_full, TC

          lar AR1, #wave      ; reset wave pointer (AR1)
wave_not_full:
          clrc INTM
          ret
.end
```

Chapter 5

Technical Data

This chapter presents the EVM technical data.

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5.1 Power-Supply Requirements

The TLV1570 EVM is designed to operate from a single, regulated, power supply.

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	2.7	5	5.5	V
Supply current (supply voltage = 5V)	I_{DD}		12		mA

5.2 Analog Input

The analog input pins of J1 are connected directly to the multiplexer inputs of the ADC. The detailed electrical specifications of the multiplexer are in the TLV1570 data sheet, literature number SLAS169.

The board can also be connected to the analog source by using J3. In this case, the value of R19 is changed to match the required input impedance. If J3 is not used, R3 should be left open**.**

The input range depends on the selected voltage reference. The default is 4 V. This can be changed by replacing D1 with a Zener diode with the required reference voltage. As the output buffer of the onboard DAC (TLV5616) has a gain of 2, the reference voltage is divided by 2 to achieve a matching output range.

With the default reference, the input range is:

Parameter		Symbol	Min	Typ	Max	Unit
Input range		V_{IN}	0		4	V
Input current	R19 ∞, multiplexer, direct	I_{IN}			±1	µA
	Multiplexer, operational amplifier			1		pA
Multiplexer on resistance		R_{MUX}			600	Ω

5.3 Analog Output

The analog output of the TLV5616 is connected directly to J1 and to JP1. R21 provides the recommended minimum load of 10 kΩ.

Chapter 6

Connector and Jumper Description

This chapter describes the EVM I/O connectors.

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6.1 Analog Interface

All the analog signals are accessible through J1.

Table 6–1. J1 Pin Assignments

Pin No.	Name	Pin No.	Name
1	CH0	2	AGND
3	CH1	4	AGND
5	CH2	6	AGND
7	CH3	8	AGND
9	CH4	10	AGND
11	CH5	12	AGND
13	CH6	14	AGND
15	CH7	16	AGND
17	AGND	18	AGND
19	OUTA	20	AGND
21	FS/OUTB	22	AGND
23	CH7	24	AGND

J3 (SMA) provides an alternative to connect the analog signal to the input of the ADC. An optional resistor (R15) can be used to match the input impedance with the source impedance. It should be removed if the multiplexer is used.

6.2 Digital Interface and Power Supply

J2 is used for the digital interface and the power supply.

Table 6–2. J2 Pin Assignments

Pin No.	Name	Pin No.	Name
3	NC	4	NC
5	NC	6	NC
7	NC	8	NC
9	NC	10	NC
11	NC	12	NC
13	/CSAD	14	/CSDA
15	NC	16	NC
17	CLKOUT	18	NC
19	DIN	20	FS
21	CLKIN	22	DOUT
23	FS	24	CLKIN
25	GND	26	3V–5V

J4 (SMA) also can be used to connect an external clock source. An optional resistor (R20) can be used to match terminate the clock line properly. It should be removed when the board is connected directly to a DSP, providing the clock signal.

Chapter 7

Schematic, Board Layout, and Parts List

This chapter contains the schematic, board layout, and parts list.

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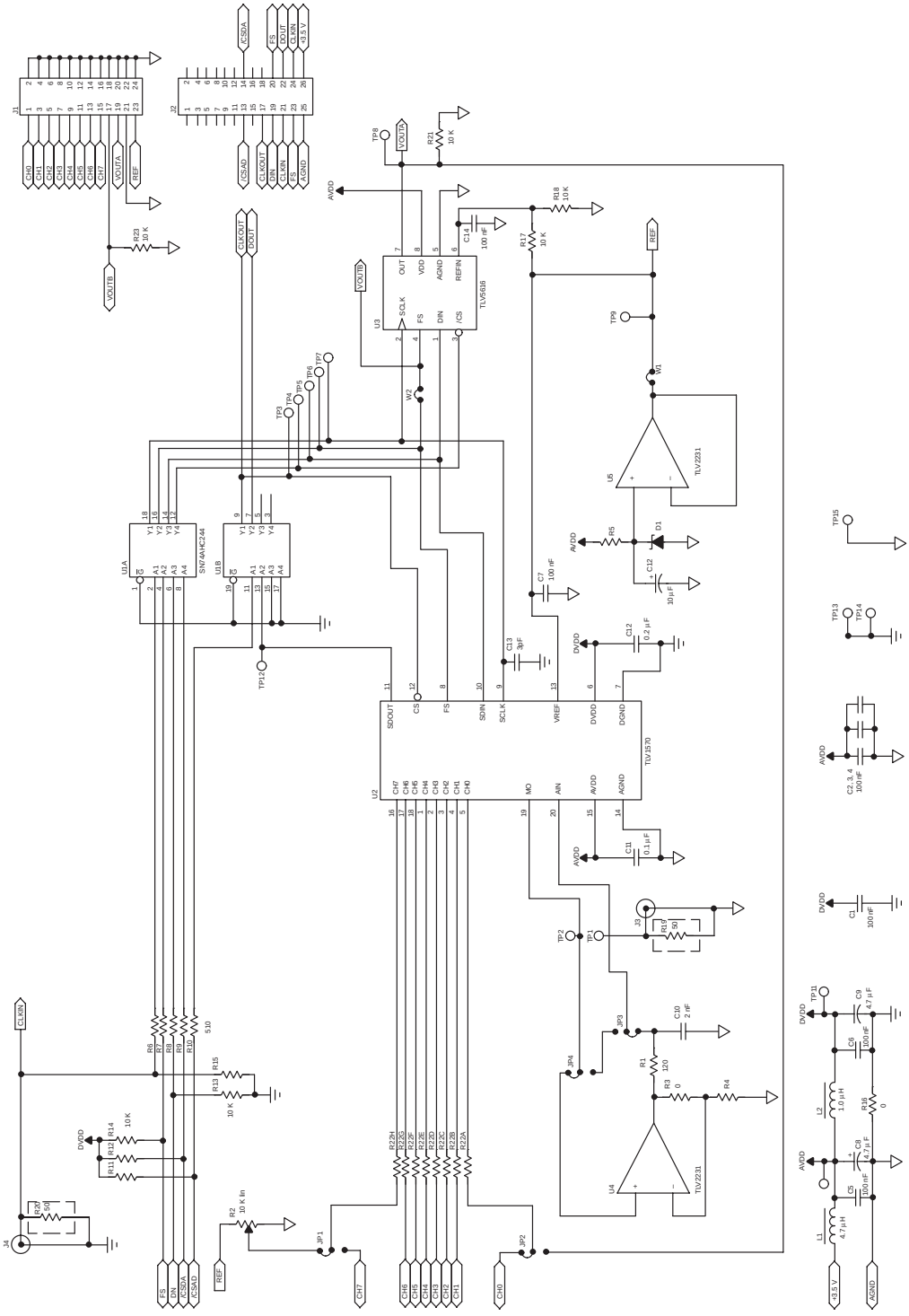
7.1 Schematic

Figure 7–1. TLV1570 EVM Schematic



7.2 Board Layout

Figure 7–2. Silkscreen Top Side

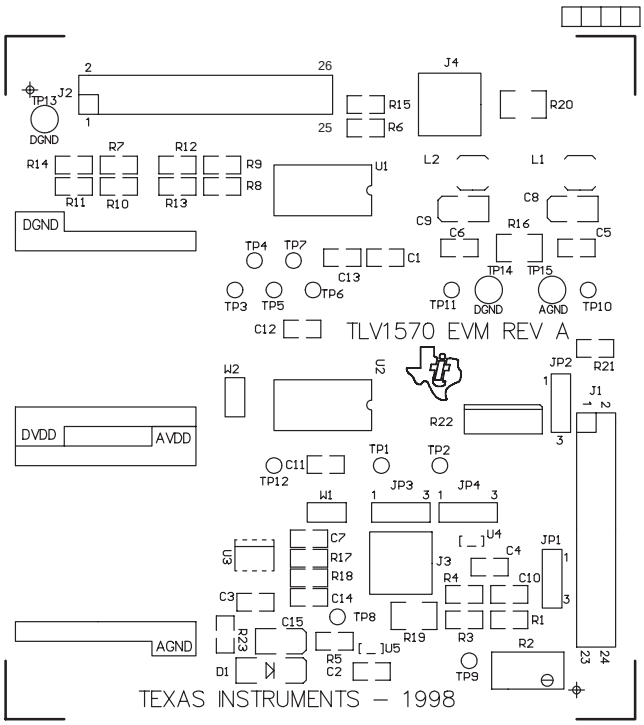


Figure 7–3. Top Layer

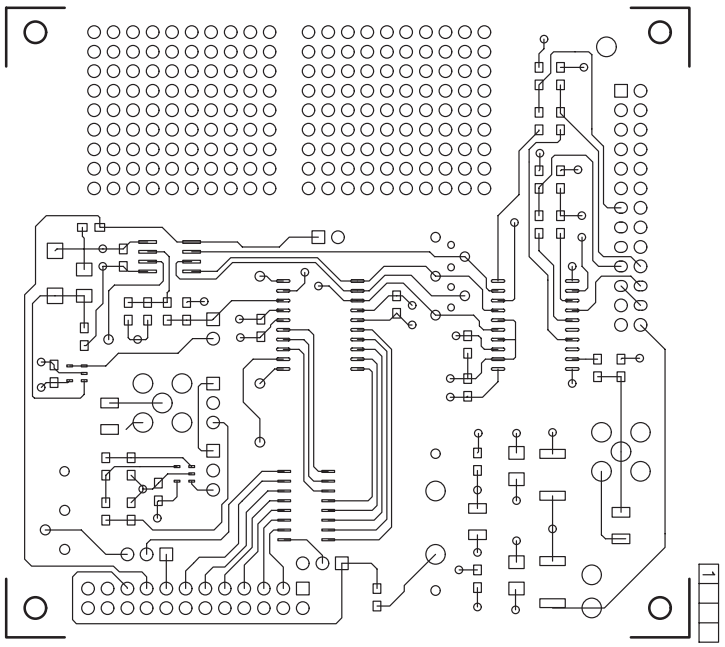


Figure 7–4. Internal Plane 1

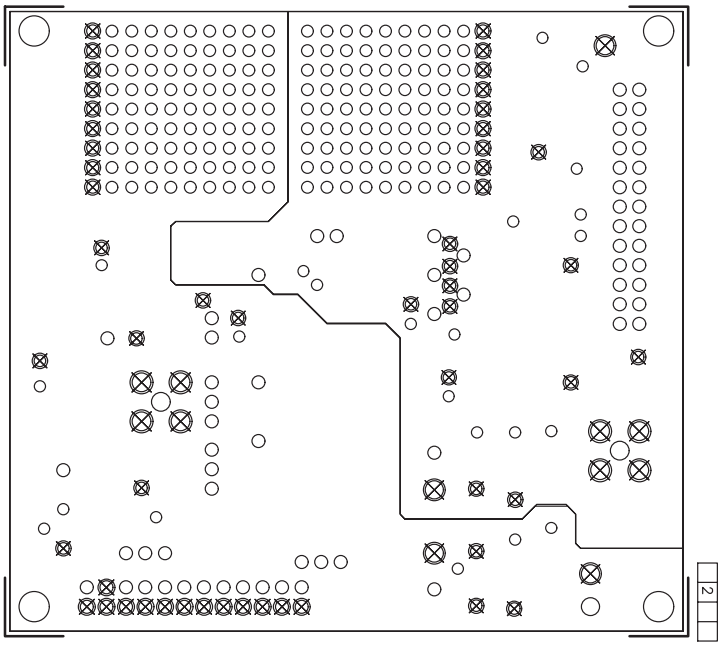


Figure 7–5. Internal Plane 2

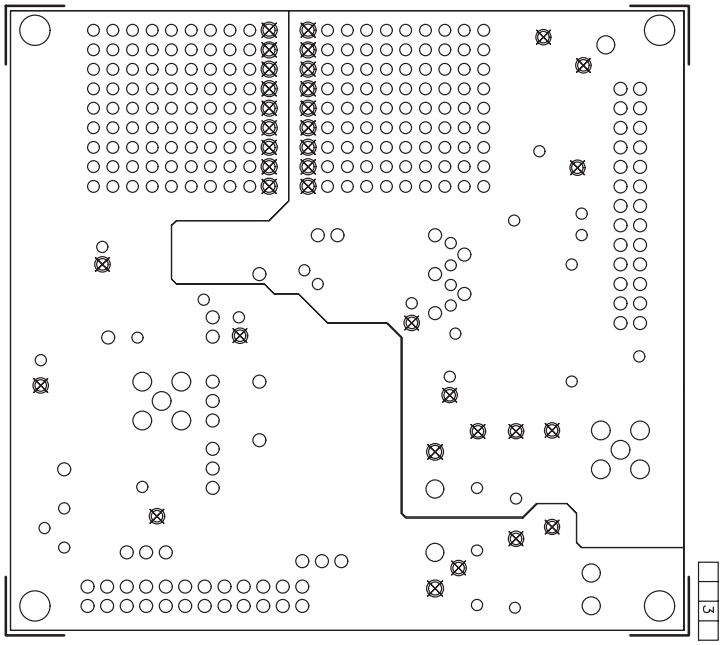
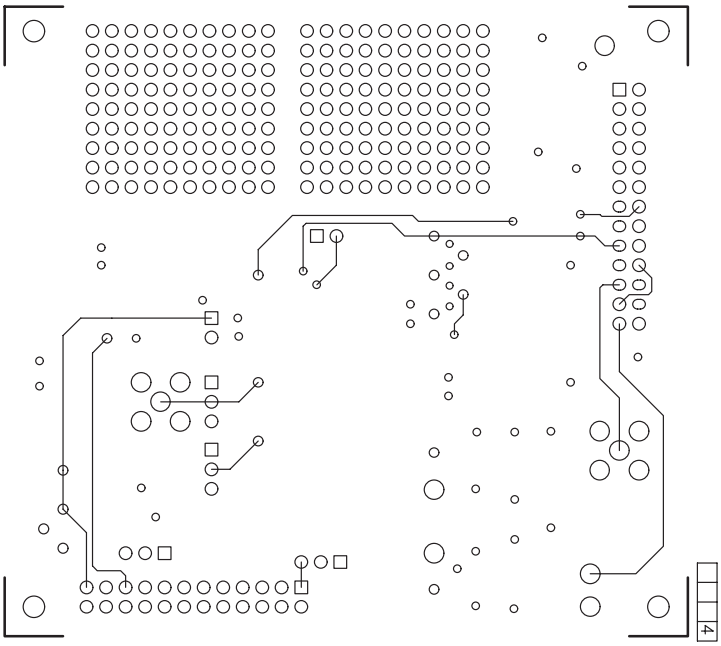


Figure 7–6. Bottom Layer



7.3 Bill of Material

Table 7–1. Parts List

Quantity	Value	Designator	Footprint	Description
1	120 Ω	R1	805	1/10-W 0805 chip resistor
1	10K	R2		Bourns 3296Y-1-103
2	0 Ω	R3, R16	805	1/10-W 0805 chip resistor
1	200 Ω	R4	805	1/10-W 0805 chip resistor
1	– –	R5	805	1/10-W 0805 chip resistor
5	510 Ω	R6, R7, R8, R9, R10	805	1/10-W 0805 chip resistor
9	10K	R11, R12, R13, R14, R15, R17, R18, R21, R23	805	1/10-W 0805 chip resistor
2	50 Ω	R19, R20	1210	1/4-W 01210 chip resistor
1	33 Ω	R22		Bourns 2NBS-16-TJ1-330
10	100 n	C1, C2, C3, C4, C5, C6, C7, C11, C12, C14	805	Multilayer ceramic
2	4.7 μF	C8, C9	3528	4.7-μF, 16-V, EIA-size 3528
1	2 nF	C10	805	Multilayer ceramic
1	2.7 pF	C13	805	Multilayer ceramic
1	10 μF	C15	3528	10-μF, 16-V, EIA-size 3528
1	Zener diode	D1	DL-41	General Semi ZM4730
2	SMA connector	J3, J4		Johnson Components 142-0701-206
4	Jumper	JP1, JP2, JP3, JP4		Berg 68217-203
1	4.7 μH	L1		Coilcraft DO1608C-472
1	1.0 μH	L2		Coilcraft DO1608C-102
12	NA	TP1–TP12		Samtec TWS-101-07-5-5
1	SN74HC244	U1	20-pin SOIC (DW)	TI SN74HC244DW
1	TLV1570	U2	20-pin SOIC (DW)	TI TLV1570DW
1	TLV5616	U3	8-pin SOIC (D)	TI TLV5616D
2	TLV2231	U4, U5	5-pin SOT (DBV)	TI TLV2231DBV
2	Jumper	W1, W2		Berg 68217-202